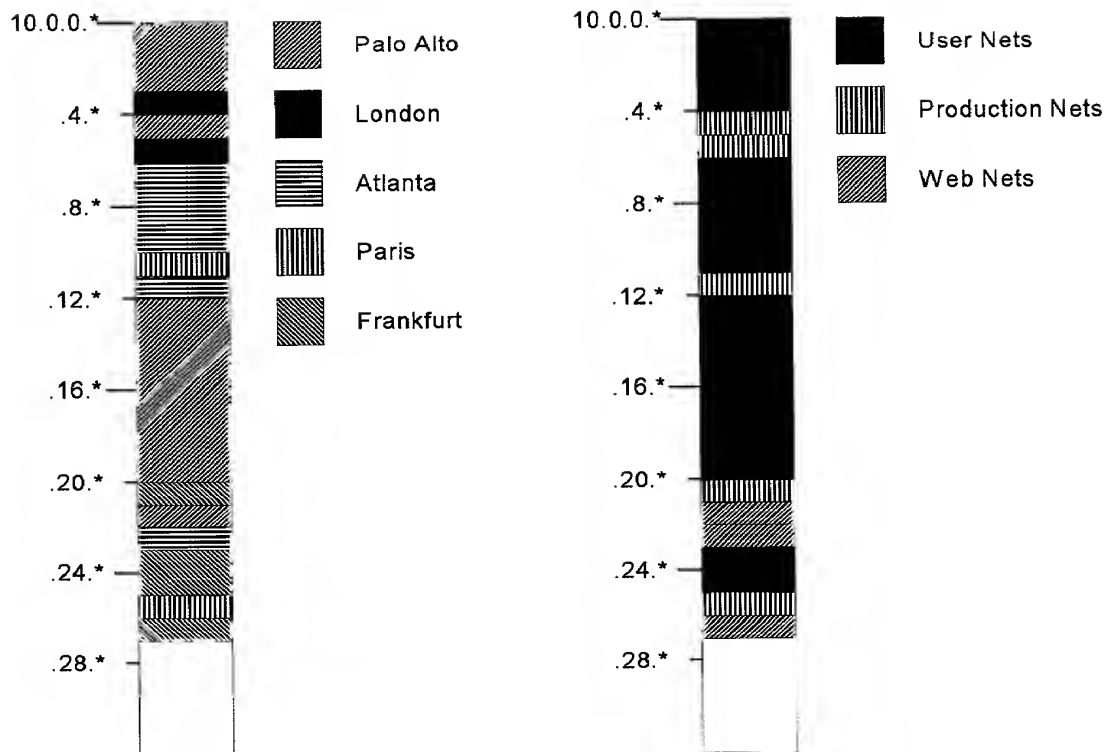


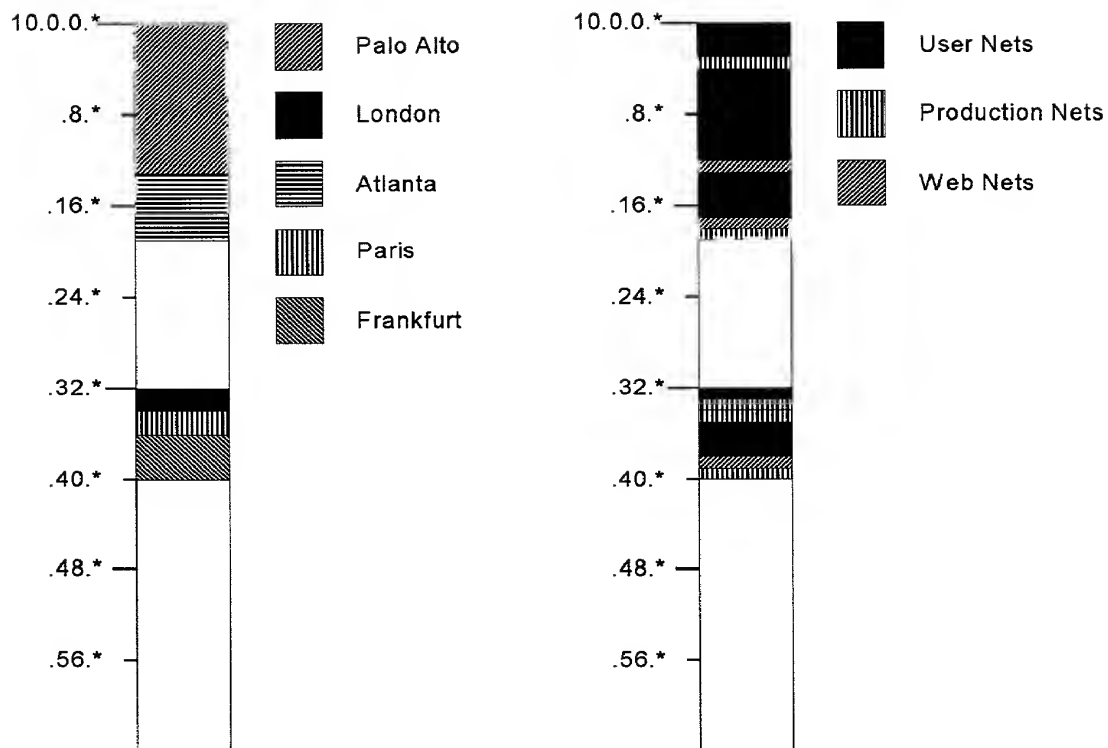
FIG. 1



PRIOR ART

FIG. 1

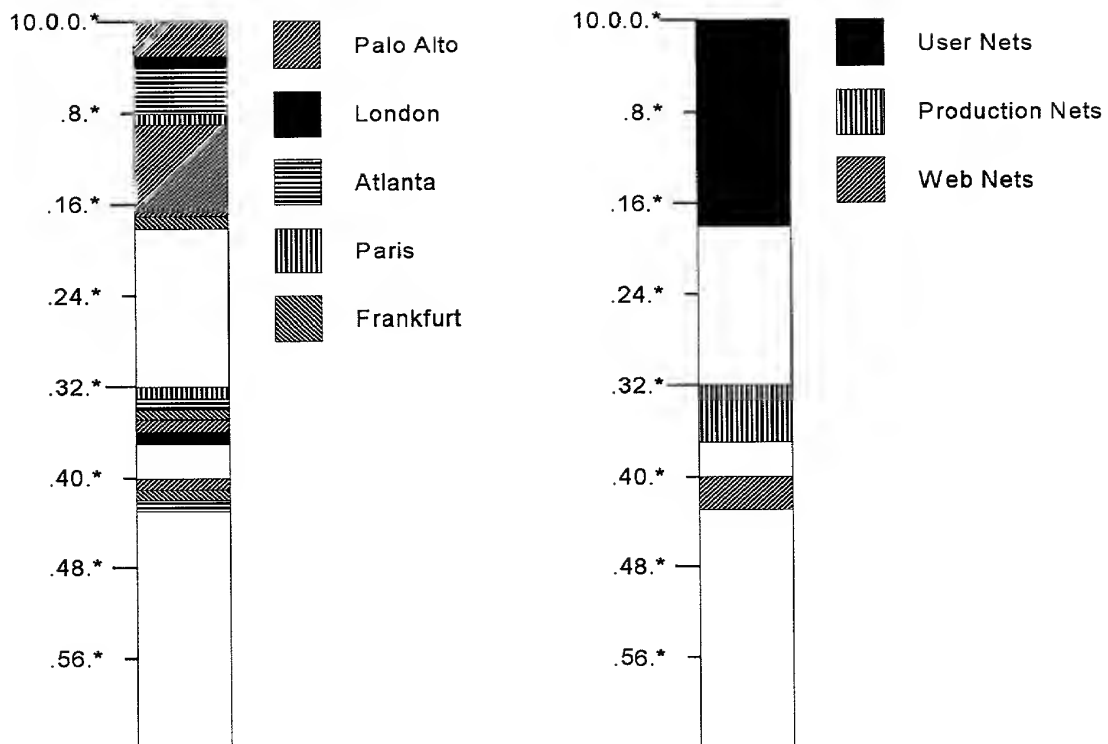
FIG. 2 is a diagram of a network topology in accordance with the present invention.



PRIOR ART

FIG. 2

FIG. 3



PRIOR ART

FIG. 3

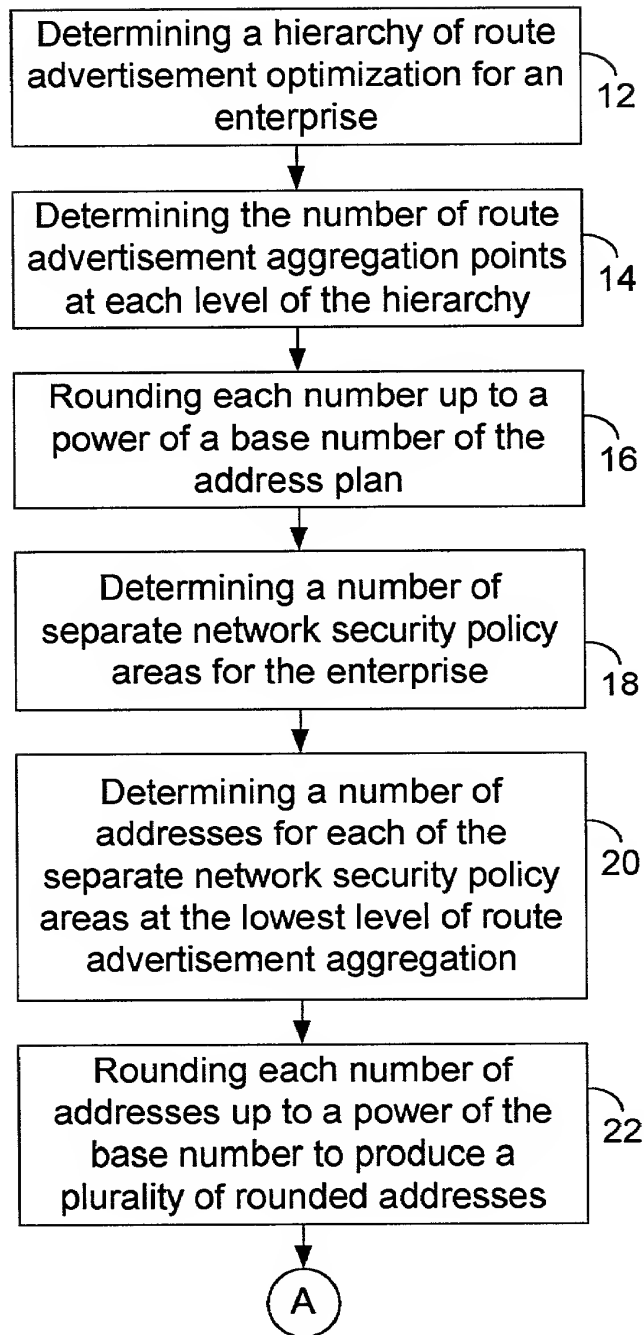


FIG. 4

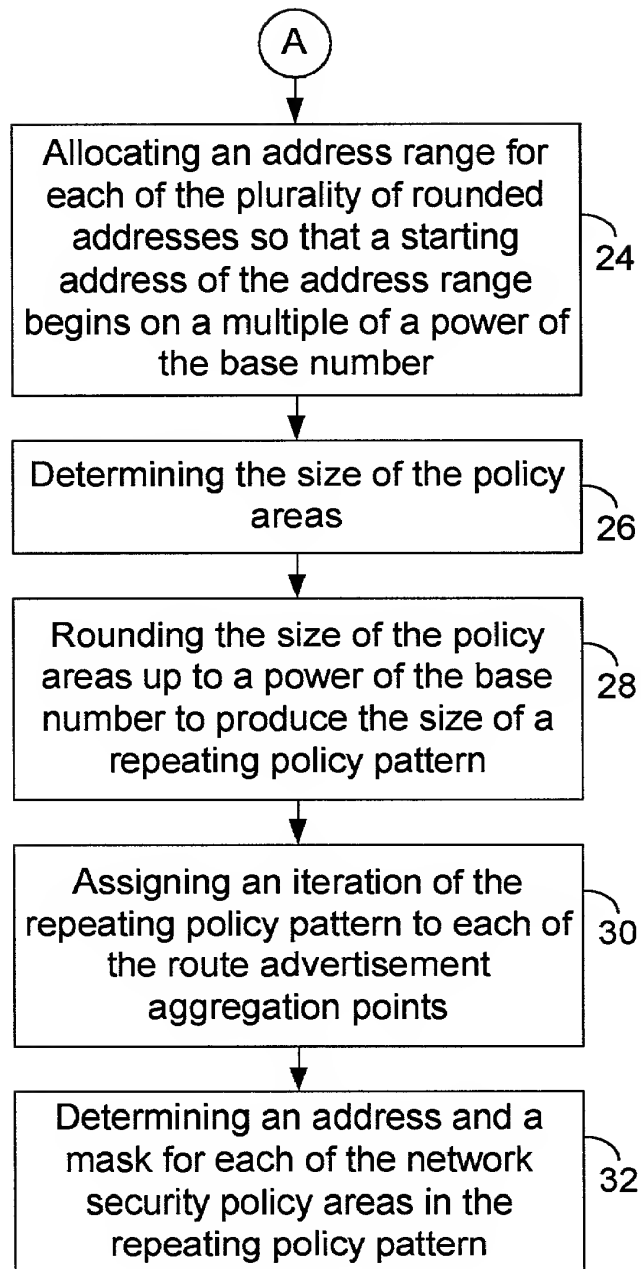


FIG. 4

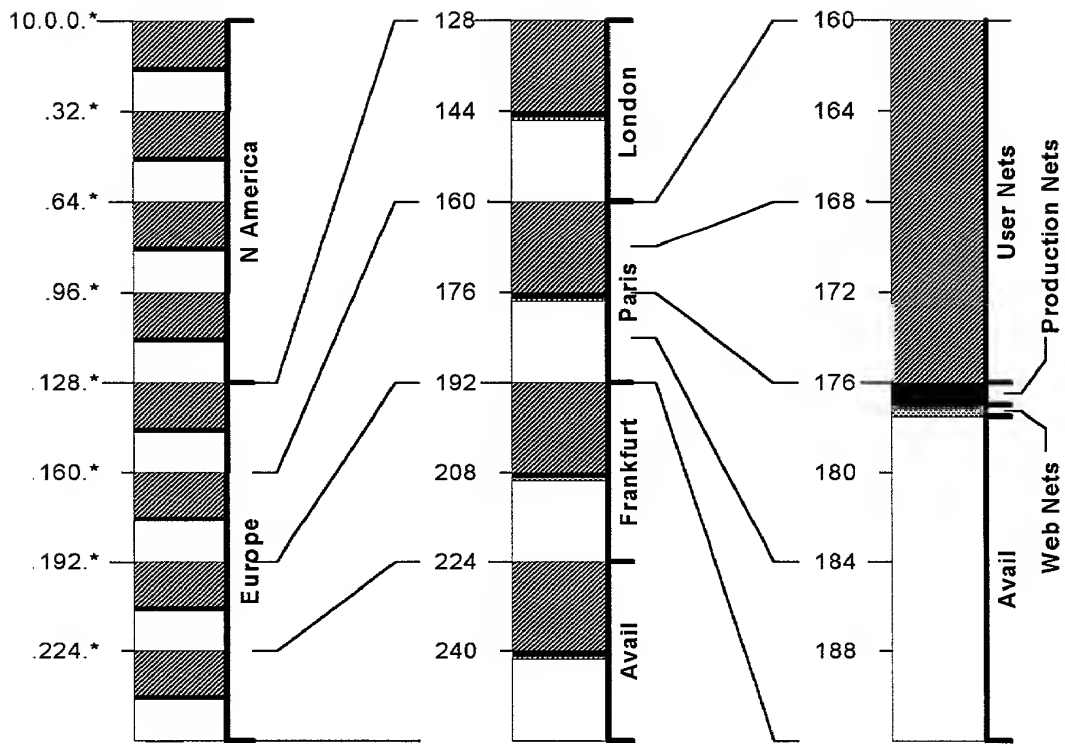


FIG. 5

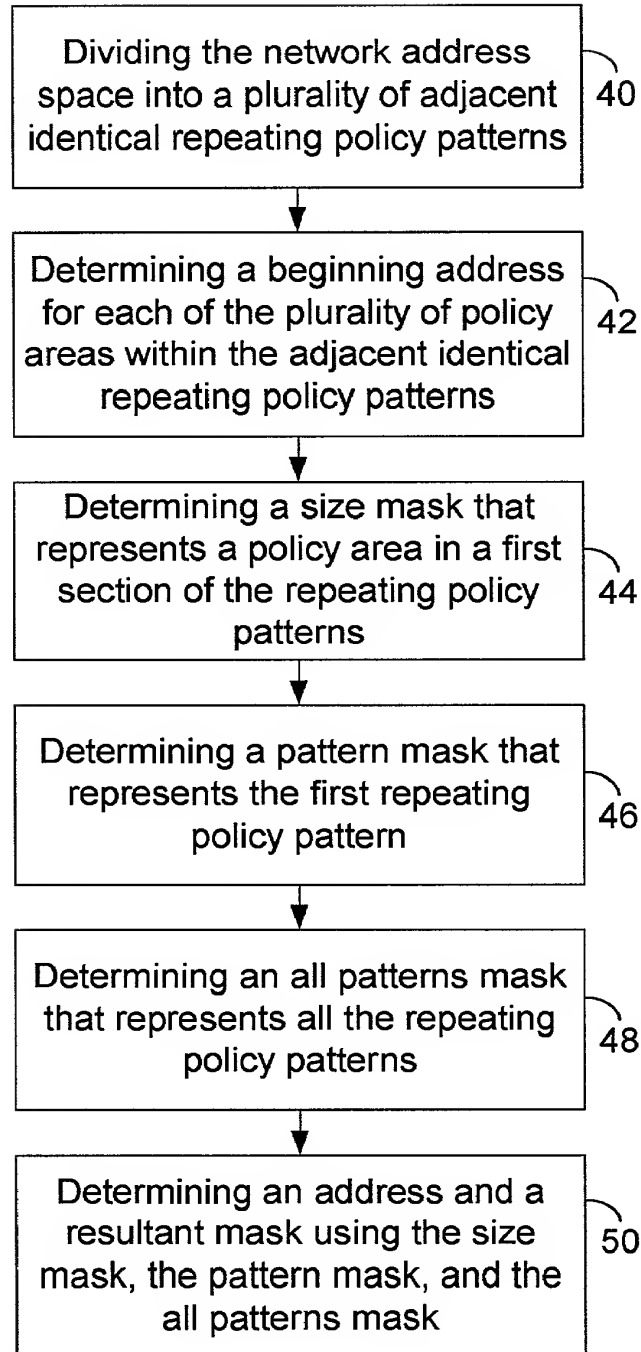


FIG. 6

FIG. 7 is a diagram illustrating a memory mask structure. The diagram shows a vertical axis on the left with addresses 0, 32, 64, 96, 128, 160, 192, and 224. A horizontal axis at the top is labeled "All Patterns Mask". A vertical line at the right is labeled "Pattern Mask". A diagonal line connects the "All Patterns Mask" label to the "Pattern Mask" label. A shaded region is shown between the diagonal line and the "Pattern Mask" label, labeled "Size Mask".

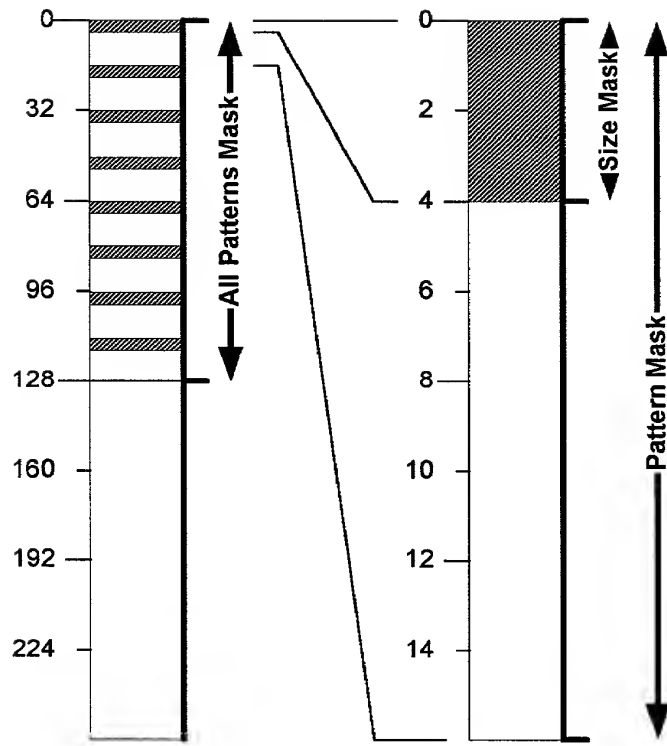


FIG. 7

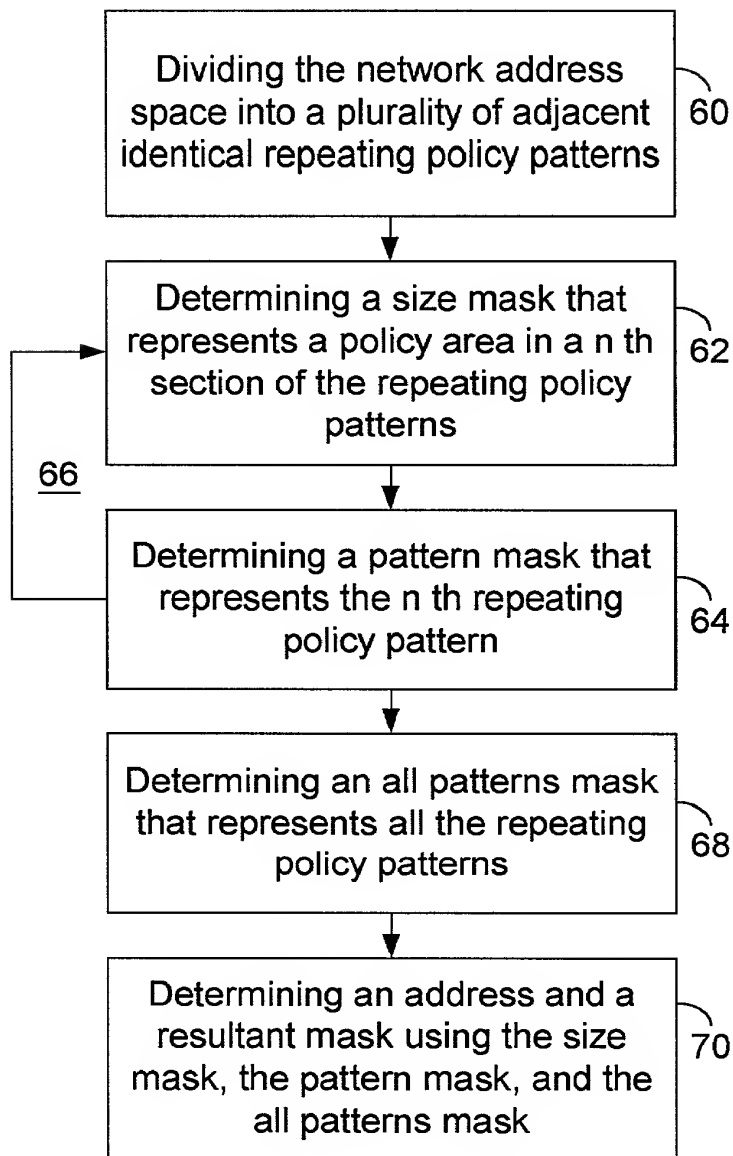


FIG. 8

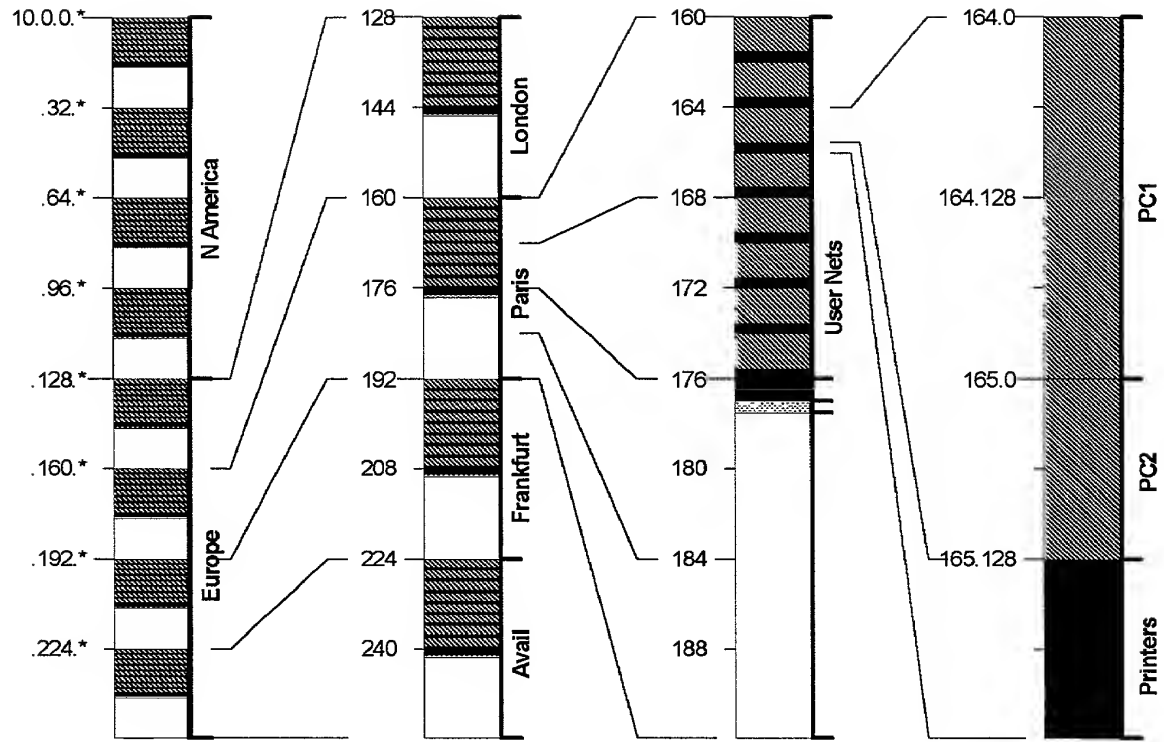


FIG. 9

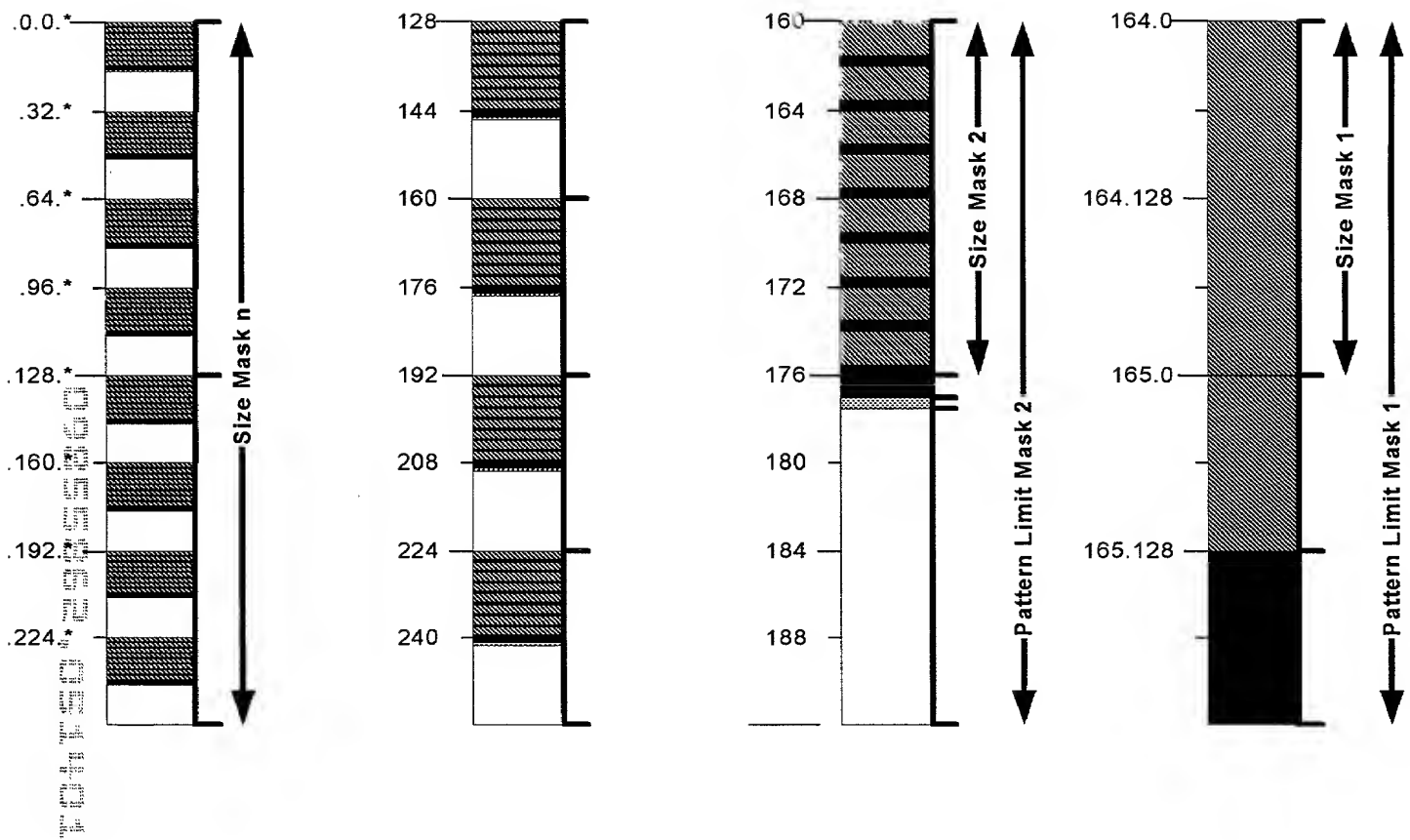


FIG. 10